PHD DEFENSE
FEBRUARY 4TH 2015

IGBT MODULE RELIABILITY

PHYSICS-OF-FAILRE BASED CHARACTERIZATION AND MODELLING

MOTIVATION

PHYSICS-OF-FAILURE (POF) BASED CONCEPTS INTEGRATION INTO DESIGN, FABRICATION, DEGRADATION ASSESSMENT, AND LIFETIME ANALYSIS IN HIGH POWER ELECTRONICS.

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SAMPLES - PRIMEPACK DESIGN

HIGH POWER INSULATED GATE BIPOLAR TRANSISTOR (IGBT) MODULES

- High power modules (1700V/1000A)
- 150A IGBT (insulated gate bipolar transistor) chips → several in parallel
- Heavy Al bond wires
- Soldered chips
- H-bridge and chopper design
- DCB with $\text{Al}_2\text{O}_3$ ceramic
- Cu baseplate (AlSiC)
OUTLINE

I. Introduction

II. Characterization techniques
   a) Accelerated testing
   b) Four-point probing
   c) Micro-sectioning

III. Lifetime estimation
   a) Coffin-Manson approach
   b) Dynamic degradation simulation

General introduction focused on power electronics

Characterization and modelling focused on power cycled IGBT modules

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INTRODUCTION

POWER DEVICES, FAILURE RATE, POWER MODULES, AND FAILURES
POWER ELECTRONICS


Guerrero et al., "Distributed Generation: Toward a New Energy Paradigm, "Industrial Electronics Magazine, IEEE, pp.52,64, March 2010
POWER MODULE FAILURES

Power module failure rate

→ Bathtub curve

Early failures – production error, transport, poor design

Random failures – external induced (cosmic rays, shocks, etc.)

Wear out – end of life wear-out (fatigue, corrosion, etc.)
SAMPLES - SECTION DESIGN

- 2x IGBTs and 2x diodes
- Al metallization (4-6μm)
- 10 Al bond wires (400μm)
- SnAg(3.5) chip solder (50-100μm)
- DCB (300/380/300μm)
FAILURE MECHANISMS

Thermo-mechanical fatigue
- Bond wire fatigue
- Metallization reconstruction
- Chip solder creep
- Baseplate solder fatigue

Thermal or mechanical induced
- Ceramic cracking
- Baseplate bending

External induced
- Corrosion
- Cosmic radiation

And so on…
FAILURE INVESTIGATION

Common failure mechanism often induce catastrophic effects.

- Explosion
- Burn-out
- Blacken

Solution:
Failure investigation prior to device failing.
CHARACTERIZATION

ACCELERATED TESTING, FOUR-POINT PROBING, AND MICRO-SECTIONING
ACCELERATED TESTING

(a) Passive thermal cycling.

(b) Active thermal cycling

Load parameters:
- Peak current $I_{\text{tot}}$: 900A
- Output frequency $f_{\text{out}}$: 6Hz
- Switching frequency $f_{\text{sw}}$: 2.5kHz
- Cooling temperature $T_{\text{SP}}$: 80degC
- DC-link voltage $V_{\text{DC}}$: 1000V

New module
- 1.3M cycles - $A_{\text{new}}$
- 2.5M cycles - $B_{20\%}$
- 3.5M cycles - $C_{40\%}$
- 4.5M cycles - $D_{60\%}$
- 5.1M cycles - $E_{80\%}$

Failed
FOUR-POINT PROBING

- Identify the weakest interface
- Electrical parameter as degree of degradation
- Degradation distribution

Section:

\[ T_{HS} \rightarrow T_{out} \]
\[ T_{out} \rightarrow T_{LS} \]

Chips:

\[ T_{HS, out} \rightarrow I_{1,2} \]

Wires:

\[ I_{1,2} \rightarrow w_{1-10} \]

Diode measurements identical with opposite direction.
WIRE CURRENT DISTRIBUTION

Clear current distribution across IGBT wires
More uniform distribution across diode wires
Change in distribution indicate wire bond degradation
Normal wear observed in all wires.

IGBTs slowly degrading as expected.

Not center wires failing first. → Consistent with thermal simulation.

Normal wear observed in all wires. LS diode failing first.

Hard failures observed suddenly in LS(2) diode.

Center wires failing first. → Consistent with thermal simulation.
MICRO-SECTIONING (M-S)

General purpose:

Separation of layered/sectionwise samples for isolation of specific areas (cross-sectional views, close inspection of subcomponents)

In our case, to access

- metallization surface for topographic and FIB inspection

- cross-sectional views of wire bonds

- cross-sectional views of semiconductor chips
M-S PROCEDURE

- Mechanical disassembly
  - Removal of housing
  - Section separation
  - Gel removal
  - Baseplate removal
  - Subcomponent disassembly
  - Fine grade polishing to reach wire interface
- Electro-chemical etching
- Microscopy investigation
BOND OPTIMIZATION

Non-terminated wire bond

Well-terminated wire bond

Grain refinement area
+ Increased strength

Large Al grains
+ Easy bonding
÷ Low strength

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INTERFACE STRUCTURE

Mapping of wire deformation + refinement + bond footprint
BOND WIRE FAILURE

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METALLIZATION RECONSTRUCTION

New

2.5MC

4.5MC
MODELLING

LIFETIME ESTIMATION AND DEGRADATION MODELLING
LIFETIME ESTIMATION

Common approach:
1. Accelerated tests
2. Model fitting
3. Extrapolation to normal operation conditions

Models:

Coffin-Manson (C-M) \[ N_f = A \Delta T_j^\alpha \]

C-M-Arrhenius \[ N_f = A \Delta T_j^\alpha \exp \left( \frac{E_A}{k_B T_{j,m}} \right) \]

SKiM63 model \[ N_f = A \Delta T_j^\alpha \exp \left( - \frac{E_A}{k_B T_{j,m}} \right) \alpha_r \beta_1 \Delta T_j + \beta_0 \left( \frac{C + t_{on}^\gamma}{C + 1} \right) f_{chip} \]

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Full 3D analysis in all steps
→ Optimization, geometry analysis (weak points, critical regions), thermal analysis, etc.

Simplified model (e.g. mean junction temperature as input)
→ Lifetime estimation or long term damage assessment
MODEL CONCEPT

Current load

Temperature field

Volumetric strain
ELECTRO-THERMAL

- Power loss calculation?
- Electro-thermal parameters of different layers?
- What elements need to be included?
- Section “symmetry”, but homogeneous power loss?
POWER LOSS AND TEMPERATURE

Switching and conduction loss contributions

\[ P_{sw,I} = f_{sw} E_{tot}(i_c, T) I_{rel}^{K_l} V_{rel}^{K_V} \]
\[ P_{con,I} = i_c(t) v_{CE}(i_c, t, T) \frac{1 + m}{2} \]
\[ P_{rec,D} = f_{sw} E_{rec}(i_c, T) I_{rel}^{K_l} V_{rel}^{K_V} \]
\[ P_{con,D} = i_D(t) v_F(i_c, t, T) \frac{1 - m}{2} \]

No gate or blocking loss included in model. Relative values are present value divided by datasheet, and \( m \) is the modulation function.

Temperature curve and distribution

\[ \nabla \cdot [k_{xyz} \nabla T(r, t)] + \frac{\partial q(\vec{r}, t)}{\partial t} = \rho c_p \frac{\partial T(\vec{r}, t)}{\partial t} \]

All calculations are carried out in time-domain with a time step size according to convergence.
BASEPLATE DISTRIBUTION

ShowerPower cooling at high flowrate
→ No BW effects on backside temperature
→ Limited backside distribution
RESISTANCE AND IMPEDANCE

Same thermal resistance → wires cause difference in thermal impedance!
Structural mechanics:
• Displacement calculation?
• Mechanical parameters of different layers?
• What elements need to be included?
• Section “symmetry”?

Bond wire fatigue:
• Separation into two types insufficient
• Lift-off consisting of multiple types of fractures (delamination, inter-, transgranular)
• Transition between types during lifetime

Metallization reconstruction
• Metallization effects – from smooth surface to porous structure
• Singular regions with highly increased load
SOLID MECHANICS APPROACH

Standard SM approach: (hysteresis)

\[ \rho \frac{\partial^2 \mathbf{u}}{\partial t^2} - \nabla \cdot \mathbf{\sigma} = F \mathbf{v} \rightarrow \mathbf{\sigma} = \mathbf{s} \]

- \( \epsilon_{th} = \alpha (T - T_{\text{ref}}) \)

- \( \dot{\epsilon}_{ij} = \dot{\epsilon}_{ij}^{(e)} + \dot{\epsilon}_{ij}^{(p)} \)

- \( F = \sigma_{VM} - \sigma_{ys} F (\sigma_{VM}, \sigma_{ys}) \leq 0 \)

- \( \dot{\epsilon}_{p} = \lambda \frac{\partial F (\mathbf{\sigma})}{\partial \mathbf{\sigma}} \)

- \( \sigma_{ys} = \sigma_{ys,0} + \delta \sigma_{ys}' \)
MODEL CONCEPT

Current load

Temperature field

Volumetric strain

\[ \delta D(x, t) = f(D, \epsilon, T) \delta T - \alpha(D, T) \delta t \]

Dislocation density increment
Damage build-up
Damage removal
DEGRADATION MODELLING

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DEGRADATION MODEL RESULTS

LS diode is stressed most due to geometry → probably fails first from fundamental wear

Specific wires are damaged additionally depending on chip, position on chip.

Wire bonds of same chip display different degradation rate

--> Consistent with micro-sectioning analysis and four-point probing results
THANK YOU FOR LISTENING!